Exploring the Potential of LSTM On Emulating Multiple-bit Fault Injection in SRAM-FPGA

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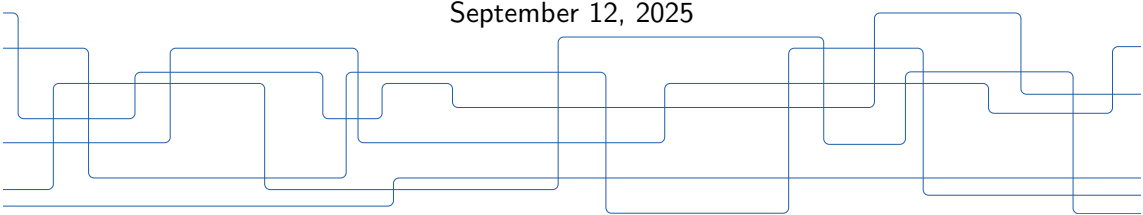

Outline

SRAM-FPGA

SRAM-FPGA is a a type of programmable IC that uses SRAM cells to configure their functionality

- High performance and cost-effective
- Support design updates with no physical hardware modifications
- Reconfigurability is attractive in space applications, nuclear reactors and underground accelerators

NASA's Mars Exploration Rover, ESA's Venus express, LHC Data acquisition system at CERN, Diagnostic systems of ITER rely on SRAM-FPGA based control systems

Single Event Upset

Single Event Upsets (SEU) are among the most prevalent radiation effects affecting SRAM-FPGA.

- A single charged particle changes the logical state of a configuration bit
- Depending on the size of the charge deposition region, a single particle can change a single bit (SBU) or multiple bits (MBU)

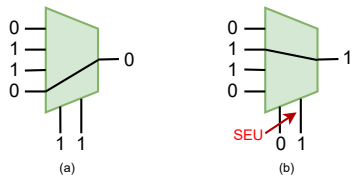

Figure: Multiplexer output (a) before SEU (b) after SEU

SEU in Configuration Memory

The configuration memory holds the static data that defines the behavior of the FPGA, such as LUT contents, multiplexer and routing switch settings.

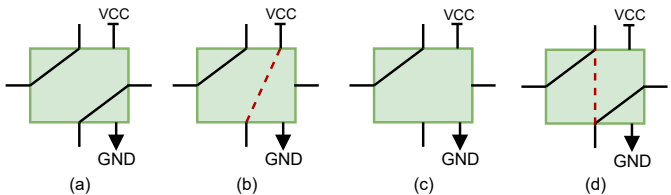

Figure: (a) Circuit before SEU. Routing changes due to SEU: (b) shorting to VCC (c) disconnected net (d) bridging nets [1]

Increase in Multiple Bit Upsets

Shrinking of CMOS devices $\rightarrow$ reduced threshold voltage $\rightarrow$ increased errors

- Triple Modular Redundancy (TMR) can be rendered ineffective when multiple modules are affected
- Error codes like SECDED becomes unreliable when multiple bits within the same codeword are corrupted simultaneously

Failure rates of 5.3% at 180 nm to 45% at 22 nm. MBUs account for 30% of SEU [2, 3]

Radiation testing

Multiple upsets are typically studied by exposing the FPGA board to charged particles in radiation chambers

- Realistic assessment of MBU effects
- Captures spatial and temporal nature of MBU

But, higher costs, limited access, lower controllability

Emulation-based Fault Injection

Offers a cost-effective and practical solution for SEU testing
Select k bits $\rightarrow$ Invert $\rightarrow$ Analyse $\rightarrow$ Clear $\rightarrow$ Repeat

- Higher controllability and reproducibility
- Highly beneficial in rapid, iterative development and test cycles.

Emulating MBU

Existing solutions extract error patterns from prior radiation data to emulate MBU

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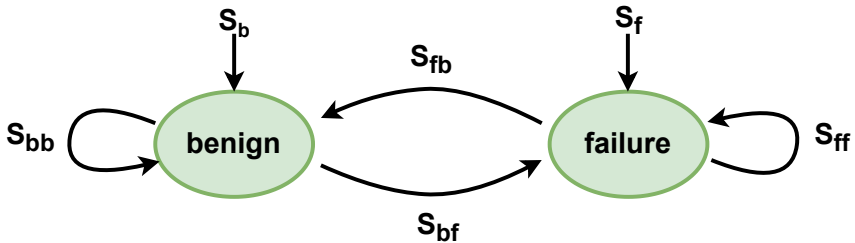
If such data is unavailable for a given device:

- Random injection campaign (exhaustive or statistically significant)
- Targeted injection of related bits through reverse-engineering techniques.

Challenges

Emulation of MBU significantly more complex than their single-bit fault emulation

In multiple-bit fault scenarios, the effects of each bit-flip can propagate and interact with subsequent faults within the same event



Challenges

- Config memory size in modern FPGAs: *Mbits* $\rightarrow$ *Gbits*
  - Xilinx Ultrascale+: 14Mbits $\times$ 3.3 seconds (FI set-up) $\rightarrow$ 534 days
  - Combinatorial explosion in testing MBU
- Reversing the layout might not be feasible
  - Layout and bitstream information is scarce
  - Significant engineering effort
  - Limited portability

Our Idea

Effective MBU emulation in FPGA requires identifying the relationships between the faults and their spatial distribution on the FPGA fabric.

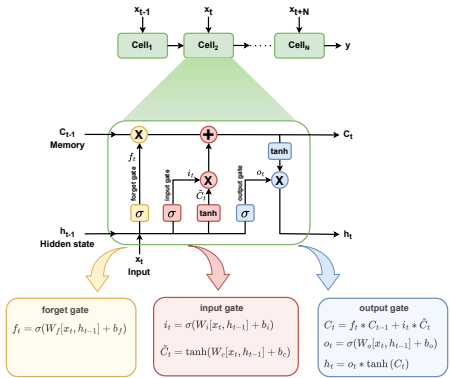
- intra-bit correlation
- upset pattern-to-frame location mappings

Can ML models map MBU patterns and predict the likelihood of bit combinations prone to failures in FPGA?

Long Short-Term Memory

Long Short-Term Memory networks are a specialized class of neural networks well-suited for modeling sequential data

- Amenable to MBU fault model as it retains and utilize information from earlier steps
- State-of-the-art performance in fault diagnosis in VLSI systems, power grids, industrial process and safety-critical applications



Modeling MBU

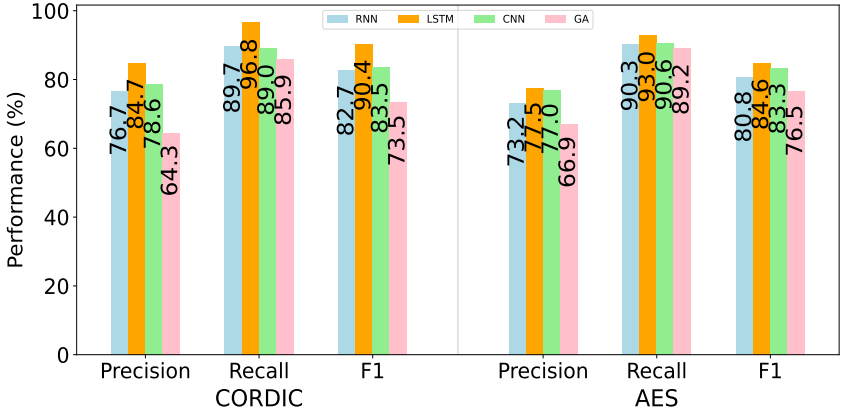
Use ML models to identify the spatial relationship between bits that transition from benign to failure states (s_{bf})

- Features: spatial hierarchy encoded in the frame address
- Training data: Fault logs $\rightarrow$ initial single bit-flip results in a benign state, but a subsequent fault induces system failure
- Evaluation: state-of-the-art models including CNN [4], GNN [5], MCTS [6] and GA [7]

Table: Frame Address Format (Xilinx Ultrascale+)

Hierarchy	Die	Block	Row	Column	Minor	Word	Bit
Bit position	[41:40]	[38:36]	[35:30]	[29:20]	[19:12]	[11:5]	[4:0]

Results



- Best performing model - LSTM $f1 = 88\%$
- MCTS and GNN models demonstrated suboptimal performance ($f1 < 50\%$)

Results

	Injections	Detected Failures (%)	Experiment Time (h)	Time Reduction (h)	Latency (ms)
Baseline	33932	100.00	33	–	–
LSTM	19768	**97.55**	20	**13**	123
CNN	20138	90.6%	20	13	139
RNN	19773	89.06	20	13	187

- LSTM 98% of the MBU in roughly 60% of the time required by the baseline (random) campaign.
- In general, ML models could detect 80% of MBU in under 20 hours vs 33 hours required by baseline

Impact

ML models show promise in MBU emulation

- Optimises fault injection campaigns by bypassing locations unlikely to cause failures
- Enables MBU modeling in the absence of radiation facilities or data
- No design flow intervention (manual floorplanning, bitstream/netlist analysis etc) or layout reverse engineering

Conclusion

- Not a replacement for radiation testing, but, offers a mechanism for early reliability assessment before radiation testing can be performed
- Future work
  - Extend to different fault models, current work uses *bit-flip* model
  - Analysis of higher-order fault patterns, current work tests double-bit upsets
  - Incorporate temporal dynamics between faults

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